ELECTRONIC CIRCUITS FOR VARIABLE BIT LENGTH, HIGH-SPEED, CLOCKLESS, BINARY ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

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ABSTRACT — It is shown that a simple circuit made of just an operational amplifier, a comparator with precision saturated output and two identical resistors can be used as the basic unit for fast, clockless, variable bit length ADC's. An inexpensive version of this circuit is discussed. It is also shown how a modified circuit can be used as the basic unit for DAC's.

The commercially available analog-to-digital converters [1] are generally of one of the following types: ramp-comparator, integrating and successive approximations. Cascade-encoder type ADC's [2, 3] while very fast have not yet lent themselves to integrated or monolithic circuit units perhaps due to the complexity of the design.

In the present work we describe a very simple circuit that can be used as the basic unit for a variable bit length ADC of the cascade-encoder type. It requires no linear gates nor clocks and lends itself to integration. The only precision components required are two identical resistors (per bit), that can be externally trimmed.

The basic circuit is indicated in Fig. 1.

If we assume that the saturated output of the comparator C is equal to E_0 (logical 1) if $V_i > E_0/2$, and equal to zero

(logical 0) if $V_i < E_0 / 2$; the output of the operational amplifier A, is (*)

$$V_0 = \begin{cases} 2\,V_i & \text{if} \quad V_i < E_0 / 2 \\ 2\,V_i - V_0 & \text{if} \quad V_i > E_0 / 2 \end{cases}$$

This means that to obtain the linear output V_0 we multiply the ratio V_i / E_0 by two and then multiply the fractional part of the number thus obtained by E_0 (it is assumed that the input voltages V_i are within the 0 to E_0 Volts range). The integer part is available as a logic signal, B, which is actually equal to the most significant bit of that number. If V_0 is fed to the input

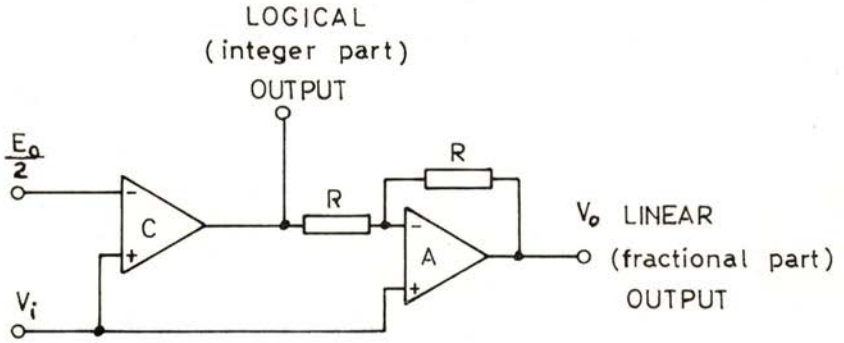

Fig. 1 — The basic circuit for building ADC's of the cascade-encoder type.

of another circuit identical to the one described, the second most significant bit can be obtained at its logical output, etc. Thus, an *n*-bit binary analog-to-digital converter can be built just by connecting in cascade *n* circuits identical to that of Fig. 1, as shown in Fig. 2.

The speed of this ADC is limited mainly by the slew rate and the settling time of the operational amplifiers and the response time of the comparators, and can thus be very fast. As soon as the first circuit processes the input signal V_i and feeds V_0 into

(*) If we consider the operational amplifier with finite gain A, common mode rejection ratio CMRR and input offset voltage e_0, V_0 will be given by $V_0 = [\,2\,V_i\ (1 + \mathrm{CMRR}^{-1}) + 2\,e_0 - E_0\,\delta\,]\ (1 + 2/A)^{-1}$ where $\delta = 1$ if $V_i > E_0 / 2$ and $\delta = 0$ if $V_i < E_0 / 2$.

the second one it is ready to start processing another input signal. Thus the different circuits in the cascade can process simultaneously successive signals. This will introduce no errors provided the logical outputs are conveniently delayed so that the digital data B_1, B_2, ... B_n corresponding to a same signal V_i arrive at the outputs at the same time. Therefore the limiting speed of this ADC is determined by that of a single stage.

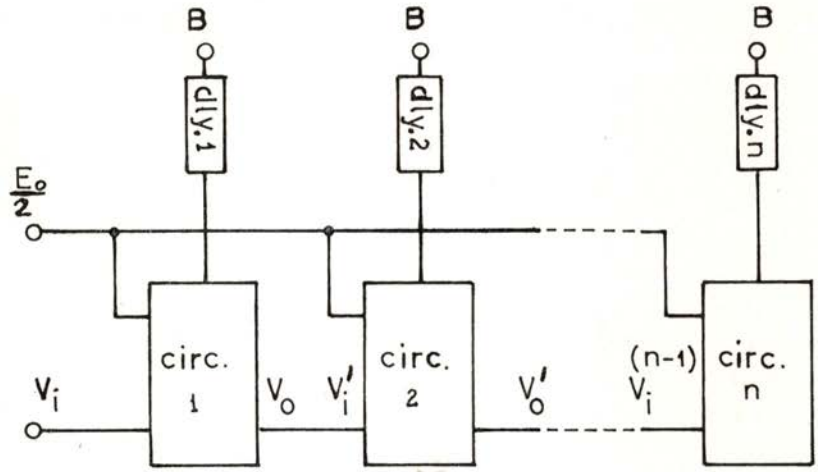

Fig. 2 — An *n* bit ADC.

The response of the basic circuit (Fig. 1) for $V_i \approx E_0/2$ was not discussed. For these cases the comparator works in the linear rather than in the saturated region and its output is somewhere between 0 and E_0. Under these circunstances the circuit does not process correctly the input V_i and gives a wrong output V_0. These cases correspond to the region of width ΔV around $E_0/2$ shown in Fig. 3. Although ΔV can be very small (of the order of 0.1 mV for a precision comparator) the errors arising in the processing are large and in general cannot be tolerated. This difficulty can be easily solved using a comparator with positive feedback (with very little backlash) or feeding the output of the comparator into a positive feedback circuit like a Schmitt trigger. Then the response of the circuit is of the type shown in Fig. 4. If the backlash ΔV_B is rather smaller than the least significant bit no appreciable errors will arise.

An experimental and inexpensive circuit of the type of that of Fig. 1 was built using a 311 comparator and a 741 operational amplifier. However as this comparator does not give a precision saturated output, it was used in a gating system to connect, through two COS / MOS bilateral switches (CD 4016), the input resistor R (10 kOhm) to a + 10 Volts (E_0) supply when the comparator output was a logical one, and to the ground potential when the comparator output was a logical zero. The experimental results show that, with no adjustments, the response function of

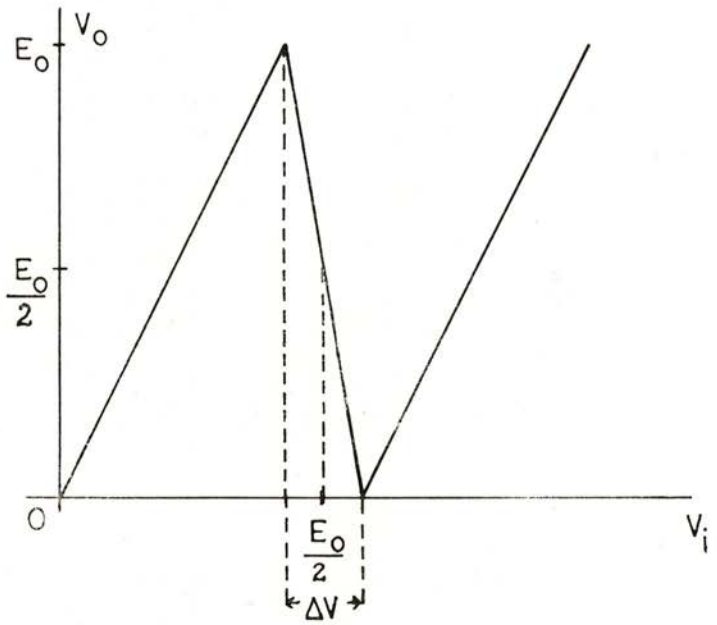

Fig. 3 — Response curve for the circuit of Fig. 1.

the circuit deviates from the theoretical function (Figs. 3 and 4) by about 2 % at the output, V_0, or by about 1 % when referred to the input. This means that ADC's with an accuracy of about 7 bits can be made with no other adjustment than the matching, in pairs, of the resistors R. The main source of error seems to arise from imperfections of the operational amplifier due to the common mode voltage applied to its positive input.

These experimental results show that it should be possible to implement in a single integrated circuit chip one or more circuits of the type of Fig. 1 using COS / MOS and MOS technologies.

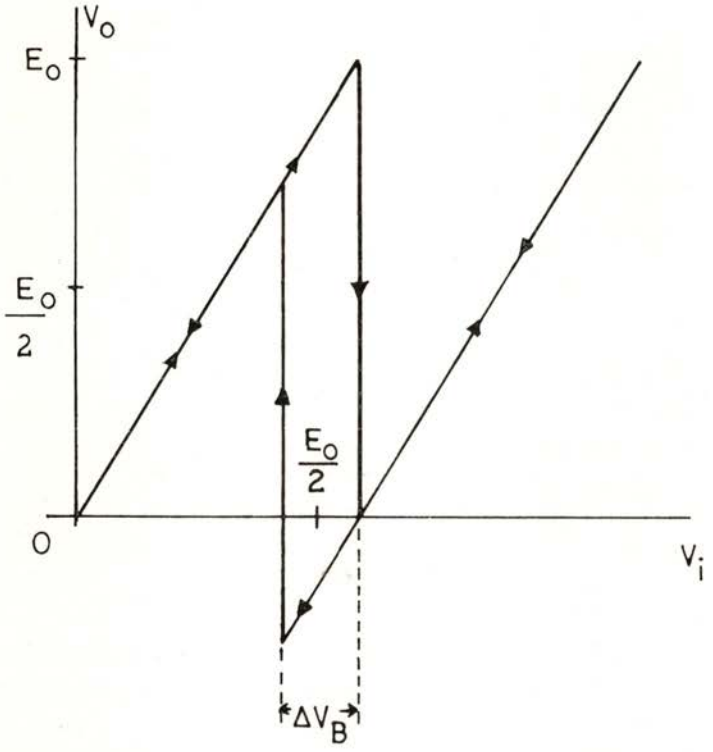

Fig. 4 — Response curve for the circuit of Fig. 1 with hysteresis.

A circuit similar to that of Fig. 1 can also be developed for digital-to-analog conversion. It is shown in Fig. 5. The amplifier with precision saturation I gives a voltage $E_1 = 0$ if bit B is zero and $E_1 = -K E_0$, where K is a scaling factor, if bit B is one. If we have various circuits like this one in cascade, short circuit to ground the input V_i of the first one, and the successive n bits of a binary number are fed at the bit inputs, B's, the linear output at the last stage is given by:

$$V_0 = (2^n B_1 + 2^{n-1} B_2 + \ldots + 2 B_n)\ K E_0$$

which is the analog conversion of the binary number. To avoid saturation of the operational amplifiers, K should be made small: for an 8 bit conversion it should be of the order of 0.001 to keep the output voltage within the 0 to E_0 range.

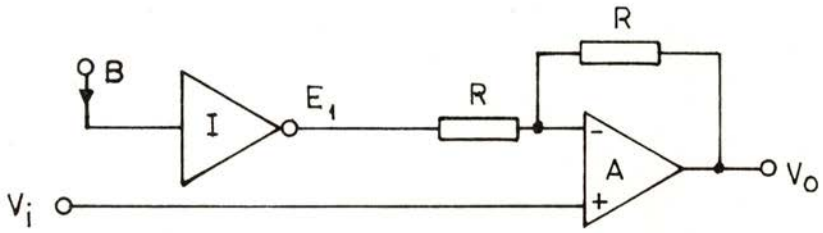

Fig. 5 — Basic circuit for building DAC's.

It is possible to have a circuit that combines the functions of the circuits of Fig. 1 and Fig. 2. With straightforward logic and with an analog switch that connects either a E_0 or a $E_1 = -K E_0$ supply, it is possible, that by the use of just a single logic signal, to have such a circuit executing either ADC or DAC functions. This circuit will not be much more complicated than that of Fig. 1 and will be thus more versatile.

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